CBCS SCHEME

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15EC61

Sixth Semester B.E. Degree Examination, Dec.2018/Jan.2019
Digital Communication

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Define Hilbert transform. What are its applications. Prove that a signal g(t) and its Hilbert transform $\tilde{g}(t)$ are orthogonal over the entire time interval $(-\infty, \infty)$. **(05 Marks)**

b. Determine the pre-envelope and complex envelope of the RF pulse defined by $x(t) = A\,\text{rect}\left(\frac{t}{T}\right)\cos(2\pi f_c t)$. **(06 Marks)**

c. Compare the power spectra of various line codes in terms of bandwidth, DC component, Noise immunity and synchronization capability, with neat sketch. **(05 Marks)**

OR

2 a. Express bandpass signal s(t) in canonical form. Also explain the scheme for deriving the inphase and quadrature components of the bandpass signal s(t). **(06 Marks)**

b. Explain with relevant expressions, the procedure for computational analysis of a bandpass system driven by a bandpass signal. **(06 Marks)**

c. What is the advantage of HDB3 code over conventional alternate mark inversion(AMI) code. Code the pattern "10100000110000110000000" using HDB3 encoding and AMI encoding. **(04 Marks)**

Module-2

3 a. Explain the geometric representation of set of M energy signals as linear combination of N orthonormal basis functions. illustrate for the case N = 2 and M = 3, with necessary diagrams and expressions. **(08 Marks)**

b. Using the Gram–Schmidt orthogonalization procedure, find a set of orthonormal basic functions to represent the three signals $s_1(t)$, $s_2(t)$ and $s_3(t)$ shown in Fig.Q3(b). also express each of these signals in terms of the set of basis functions. **(08 Marks)**

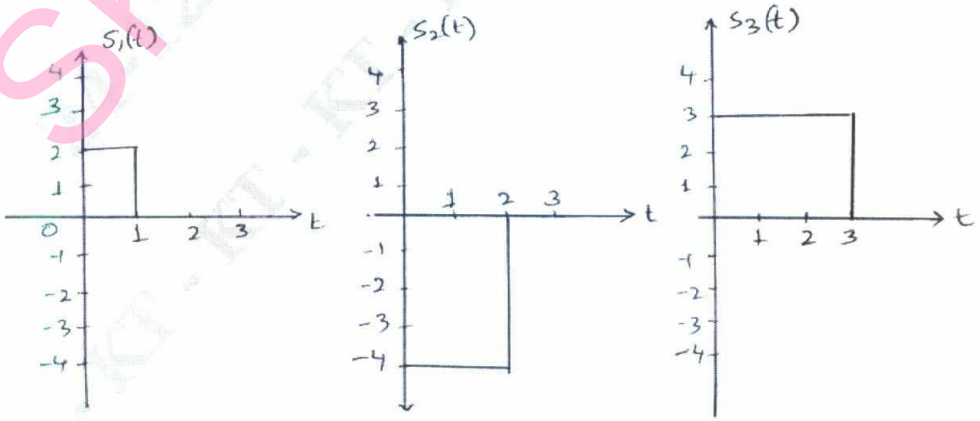

Fig.Q3(b)

OR

4 a. Explain the correlation receiver with neat diagrams and explanation of detector and the maximum –linklihood decoder blocks. **(08 Marks)**

b. Explain the matched filter receiver. Obtain the expression for the impulse response of the matched filter. **(08 Marks)**

Module-3

5 a. Derive the expression for error probability of binary PSK using coherent detection. **(06 Marks)**

b. Binary data are transmitted over a microwave link at the rate of 10^6 bits/sec and the power spectral density of the noise at the receiver input is 10^{-10} ω/Hz. find the average carrier power required to maintain an average probability of error $Pe \leq 10^{-4}$ for the following cases.
Binary PSK using coherent detection
DPSK
Note : take $erfc(2.63) = 2 \times 10^{-4}$, $Q(3.7) = 10^{-4}$. **(06 Marks)**

c. Define bandwidth efficiency. Tabulate and comment on the bandwidth efficiency of M-ary PSK signals for different values of M. **(04 Marks)**

OR

6 a. With neat diagram and expressions, explain binary FSK generation and non-coherent detection scheme. **(06 Marks)**

b. Explain the generation and optimum detection of differential phase – shift keying with neat block diagram. **(06 Marks)**

c. What is the advantage of M-ary QAM over M-ary PSK system? Obtain the constellation of QAM for M = 4 and draw signal space diagram. **(04 Marks)**

Module-4

7 a. With a neat block diagram, explain the digital PAM transmission through band limited baseband channels. Also obtain the expression for inter symbol interference. **(06 Marks)**

b. Explain the modified duo-binary signaling scheme, with pre-coding. Illustrate the encoding for the binary sequence "011100101". Assume previous pre-coder outputs as 1. **(07 Marks)**
With neat diagram, explain the timing features pertaining to eye diagram and it interpretation for baseband binary data transmission system. **(03 Marks)**

OR

8 a. With neat sketches and expressions, explain raised cosine spectrum solution to reduce ISI. **(06 Marks)**

b. What is the advantage of controlled ISI partial response signaling scheme? With block diagram, explain the duo-binary encoder with pre-coder. Mention the frequency response, impulse response and its features. **(06 Marks)**

c. With neat diagram and relevant expressions, explain the concept of adaptive equalization. **(04 Marks)**

Module-5

9 a. Explain the working of Direct Sequence Spread Spectrum transmitter and receiver with neat diagram, waveform and expressions. **(08 Marks)**

b. A slow frequency Hopped/MFSK system has the following parameters,
   i) The number of bits/MFSK symbol = 4
   ii) The number of MFSK symbols per hop = 5
   iii) Calculate the processing gain of the system in decibels. **(03 Marks)**

c. List and briefly explain any 3 applications of direct sequence spread spectrum. **(05 Marks)**

OR

10 a. With a neat block diagram, explain frequency Hopped spread spectrum technique. Explain the terms chip rate, Jamming Margin and processing gain. **(08 Marks)**

b. What is a PN sequence? Explain the generation of maximum-length sequences (ML-sequence). What are the properties of ML sequences? **(04 Marks)**

c. In a DS/BPSK system, the feedback shift register used to generate the PN sequence has length m = 19. The system is required to have an average probability of symbol error due to externally generated interfering signals that does not exceed 10^{-5}. Calculate the following system parameters in decibels :
   i) Processing gain
   ii) Antijam margin
   (Assume Q(4.25) = 10 –5 or erfc(3) = 2×10^{-5}). **(04 Marks)**

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15EC62

Sixth Semester B.E. Degree Examination, Dec.2018/Jan.2019
ARM Microcontroller and Embedded Systems

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain architectural features of cortex M3 with block diagram. **(07 Marks)**
b. Briefly describe the special registers of cortex M3. **(06 Marks)**
c. What is stack and what are the instructions to access stack? **(03 Marks)**

OR

2 a. Briefly discuss features of built in nested vector interrupt controller. **(08 Marks)**
b. Write a short note on :
i) Debugging support
ii) Interrupts and exceptions supported by cortex M3. **(08 Marks)**

Module-2

3 a. Explain memory map of cortex M3 with diagram. **(08 Marks)**
b. Write C language program to toggle an LED with small delay in cortex M3. **(05 Marks)**
c. Explain the 32 bit multiply instruction set. **(03 Marks)**

OR

4 a. Explain arithmetic instruction set with example. **(07 Marks)**
b. Briefly explain shift and rotate instructions with diagrams. **(07 Marks)**
c. Explain working of following instructions :
i) CMP ii) TST iii) CMN iv) REV. **(02 Marks)**

Module-3

5 a. Explain the sequence of operations for communicating with an I2C slave device. **(08 Marks)**
b. Write the differences between :
i) RISC and CISC
ii) Harvard architecture and Von Neumann architecture. **(08 Marks)**

OR

6 a. Briefly explain PLDs and types of PLDs. **(06 Marks)**
b. Write short note on :
i) Optocoupler
ii) COTS. **(08 Marks)**
c. Explain working of DRAM. **(02 Marks)**

Module-4

7	a.	List and explain characteristics of an embedded system.	(06 Marks)
	b.	Briefly describe any two operational and two non operational quality attributes.	(08 Marks)
	c.	Define and classify electronic control units.	(02 Marks)

OR

8	a.	Discuss fundamental issues in hardware software co-design.	(08 Marks)
	b.	Differentiate between DFG and CDFG with example.	(04 Marks)
	c.	Explain different types of serial interface buses deployed in automatic embedded application.	(04 Marks)

Module-5

9	a.	Define process and explain process states and states transition diagram.	(07 Marks)
	b.	Explain functional requirements to be analysed in selection of an RTOS.	(06 Marks)
	c.	Differentiate between threads and process.	(03 Marks)

OR

10	a.	Explain round robin scheduling technique.	(03 Marks)
	b.	Three process with process IDs P1, P2, P3 with estimated completion time 10, 5, 7 ms respectively enters ready queue together. A new process P4 with estimated completion time 2ms enters ready queue after 2ms. Calculate waiting time, turnaround time and average turnaround time with help of preemptive SJF scheduling.	(10 Marks)
	c.	Explain concept of pipe for IPC.	(03 Marks)

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15EC63

Sixth Semester B.E. Degree Examination, Dec.2018/Jan. 2019
VLSI Design

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Mention any two differences between CMOS and Bipolar technology. **(02 Marks)**

b. Write all the mask steps of p-well process. **(06 Marks)**

c. With neat diagrams, explain the cut off, linear and saturation regions formation in MOSFET with different values of V_{gs} and V_{ds}. **(08 Marks)**

OR

2 a. Explain body effect as non ideal IV effects of MOSFET. **(03 Marks)**

b. Explain Noise margin, with respect to CMOS inverter. **(05 Marks)**

c. Explain the steps of n-MOS fabrication with neat diagram. **(08 Marks)**

Module-2

3 a. With a neat diagram, explain λ - rules for buried and butting contact and show thE cross sectional view of same. (white any one structure burreid contact). **(08 Marks)**

b. Estimate the rise time and fall time of a CMOS inverter and summarise the result. **(08 Marks)**

OR

4 a. Define sheet resistance, with equation. **(02 Marks)**

b. Calculate the area capacitance of the layer below [Refer Fig.Q4(b)] :

Fig.Q4(b)

i) If the layer is metal – 1 and relative capacitance value is 0.075 □C_g

ii) if the layer is polysilicon and relative capacitance value is 0.1□C_g. **(06 Marks)**

c. Write the schematic and stick diagram for Boolean expression $y = \overline{(a + bc)}$.(implement using CMOS logic). **(08 Marks)**

Module-3

5 a. Design a 4bit, 4 × 4 barrel shifter. Write the nMOS implementation and strategy for the same. **(08 Marks)**

b. Explain carry select adder with neat block diagram. **(08 Marks)**

OR

6 a. Define regularity. **(02 Marks)**

b. Derive the scaling factor for the device parameter :
   i) Parasitic capacitance
   ii) Channel resistance
   iii) Gate delay. **(06 Marks)**

c. Implement the ALU functions like EX-OR, EX-NOR AND and OR operations with an adder. Write the block diagram of 4-bit ALU using adder element. **(08 Marks)**

Module-4

7 a. Explain the following logics :
   i) Clocked CMOS logic
   ii) n-p CMOS logic. **(08 Marks)**

b. Explain parity generator, with the nMOS implementation of parity generator with stick diagram. **(08 Marks)**

OR

8 a. Explain Pseudo-nMOS logic. Find Z_{pu}/Z_{pd} when $V_{inr} = 0.5V_{DD}$, $V_{tn} = |V_{tp}| = 0.2V_{DD}$, $V_{DD} = 5V$ and $\mu_n = 2.5\mu p$. **(08 Marks)**

b. Explain the 4-way data selector (multiplexer) with Boolean equation and nMOS based stick diagram. **(08 Marks)**

Module-5

9 a. Write the system timing considerations. **(08 Marks)**

b. Explain logic verification principle. **(08 Marks)**

OR

10 a. Explain three transistor dynamic RAM with neat circuit and stick diagram. **(06 Marks)**

b. What are design manufacturability. **(10 Marks)**

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15EC64

Sixth Semester B.E. Degree Examination, Dec.2018/Jan.2019
Computer Communication Networks

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

1 a. Show the encapsulation and decapsulation representation in the TCP/IP model and explain. **(06 Marks)**

b. Define framing, explain role of bit stuffing in a framing. **(04 Marks)**

c. Mention the different network topology. List out advantages and disadvantages of each topology. **(06 Marks)**

OR

2 a. What are five components involved in data communication? Explain with a suitable diagram. **(05 Marks)**

b. Demonstrate stop and wait protocol by considering acknowledgement, timer and sequence no with the help of flow diagram. **(06 Marks)**

c. Describe link layer addressing with suitable illustration. **(05 Marks)**

Module-2

3 a. A ALOHA network transmits 200 bit frame using a shared channel with a 200 kbps band width. Find the through put of pure and slotted ALOHA if the system produces 500 frame per second. **(06 Marks)**

b. Describe the frame format of IEEE 802.3 Ethernet. What are minimum and maximum length of frame? **(07 Marks)**

c. Identify unicast, multicast and broad cast from the following MAC addresses:
4A : 30 : 10 : 21 : 10 : 1A
47 : 20 : 1B : 2E : 08 : EE
FF : FF : FF : FF : FF : FF. **(03 Marks)**

OR

4 a. A network using CSMA/CD has a band width of 10 Mbps. If the maximum propagation time is 25.6μs. What is the minimum size of the frame? **(05 Marks)**

b. Explain polling technique with suitable illustration. **(06 Marks)**

c. In the standard Ethernet with the transmission rate of 10 Mbps, length of cable is 2500 mt and frame size is 512 bits. The propagation speed of a signal in a cable is 2×10^8 m/s. Find efficiency of standard Ethernet. **(05 Marks)**

Module-3

5 a. Explain the following connecting devices: i) Hub ii) Link layer switch iii) Router. **(06 Marks)**

b. Define two types of Bluetooth networks. **(06 Marks)**

c. Differentiate between data gram network and virtual circuit network. **(04 Marks)**

OR

6 a. Define IEEE 802.11 addressing mechanism for four cases. **(06 Marks)**

b. Give a note on virtual LAN. **(05 Marks)**

c. An organization is granted a block of address with the beginning addresses 14.24.74.0/24. The organization need to have 3 sub blocks of addresses to use in its three subnets: one sub block of 10 addresses, one sub block of 60 addresses, and one sub block of 120 addresses. Design the sub blocks. **(05 Marks)**

Module-4

7 a. Give a brief overview of IPV4 datagram. **(10 Marks)**

b. Find the shortest path from source 'A' to destination 'G' from given graph as shown in the Fig.Q.7(b) using the Dijkstra algorithm. **(06 Marks)**

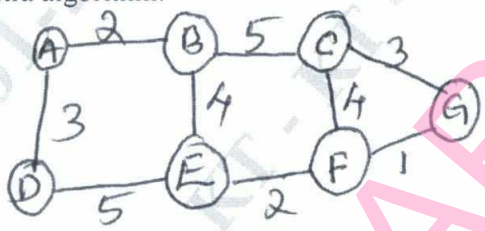

Fig.Q.7(b)

OR

8 a. Explain three phases of communication between a remote host and mobile host. **(08 Marks)**

b. Explain distance-vector-routing using a Bellman Ford algorithm providing a suitable illustration. **(08 Marks)**

Module-5

9 a. Describe connectionless and connection – oriented services provided by the transport layer. **(08 Marks)**

b. Discuss TCP segment. **(08 Marks)**

OR

10 a. Demonstrate Go-back-n protocol with a forward channel is reliable but in the reverse channel, if an acknowledgment is delayed or lost. **(06 Marks)**

b. Explain a TCP connection establishment using three way hand shaking. **(10 Marks)**

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15EC663

Sixth Semester B.E. Degree Examination, Dec.2018/Jan.2019
Digital System Design using Verilog

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain with illustration, a simple design methodology followed in IC industries. **(08 Marks)**

b. Explain the following constraints imposed in real world circuits :
i) Noise margin ii) propagation delay. **(03 Marks)**

c. Develop a verilog model for a 7–segment decoder, include an additional input, blank, that overrides the BCD i/p and causes all segments not to be lit. **(05 Marks)**

OR

2 a. Develop a verilog module of a debouncer for a push button switch that uses a debounce interval of 10ns. Assume the system clock frequency is 50 MHz. **(06 Marks)**

b. Design and develop a circuit and verilog module for modulo 10 counters. **(06 Marks)**

c. What is the distinction between a Moore and Mealy finite state machine? **(04 Marks)**

Module-2

3 a. Write a symbol for basic memory component and explain its parts. **(06 Marks)**

b. Explain about the multiport memories. **(06 Marks)**

c. Compute the 12-bit ECC word corresponding to the 8-bit data word "0110001". **(04 Marks)**

OR

4 a. Design a 64 K × 16 bit composite memory using 16K × 8 bit component. **(08 Marks)**

b. What is the difference between asynchronous static RAM and synchronous static RAM? **(06 Marks)**

c. Using a Hamming code, how many check bits are required for single error correction and double error detection for 4-bit data word? **(02 Marks)**

Module-3

5 a. Design a priority encoder that has 16 inputs, i[0 : 15]; a 4-bit encoded output, z[3 : 0] and a valid output ie. '1' when any input is '1'. Input i[0] has the highest priority and i[15] is the lowest priority. **(08 Marks)**

b. Explain the concept of differential signaling. How does differential signaling improve noise immunity? **(08 Marks)**

OR

6 a. What are the purpose of logic blocks and I/O blocks in FPGA? **(06 Marks)**

b. Explain different types of PCB design. **(03 Marks)**

c. Explain with a neat diagram of the internal organization of a CPLD. **(07 Marks)**

Module-4

7 a. What are the purpose of following in an I/O controller : i) input register ii) output register iii) control register iv) status register. **(06 Marks)**

b. Explain neatly the designing a R-string DAC. **(05 Marks)**

c. Explain about tristate buses and weak drive. **(05 Marks)**

OR

8 a. Design and develop a verilog code for an input controller that has 8-bit binary-coded input from a sensor. The value can be read from an 8-bit input register. The controller should interrupt the embedded Gumnut. When input value changes the controller is the only interrupt in the system. **(08 Marks)**

b. What are the serial input standards? Briefly explain each. **(08 Marks)**

Module-5

9 a. Explain the design flow of hardware/software co-design. **(10 Marks)**

b. Briefly describe techniques used in power optimization. **(06 Marks)**

OR

10 a. What is the distinction between logical partition and physical partition? **(08 Marks)**

b. Explain Built-In–Self–Test (BIST) techniques. **(08 Marks)**

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